UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,934	10/15/2001	Hajime Akimoto	520.36114CX1	2676

20457 7590 12/13/2002

ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

EXAMINER
LIANG, REGINA

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 13

Application Number: 09/975,934
Filing Date: October 15, 2001
Appellant(s): AKIMOTO ET AL.

Melvin Kraus
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/25/2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-15 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

No prior art is relied upon by the examiner in the rejection of the claims under appeal.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-15 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-9, 11-16 of prior U.S. Patent No. 6,329,973. This is a double patenting rejection.

The term "AND functional circuit" in the independent claims of the present application and the term "AND logical circuit" in the allowed independent claims of the prior U.S. Patent No. 6,329,973 are directed to the same AND gate circuit, therefore, claims 1-15 of the present application are claiming the same invention as that of claims 1-9, 11-16 of prior U.S. Patent No. 6,329,973.

(11) Response to Argument

Appellants' remarks regarding the 101 double patenting are not persuasive. Appellants alleges "the term AND functional circuit recited in independent application claims 1, 10 and 14-15 is not limited to an implementation with a digital circuit, but means any circuit which performs an AND function, and may be implemented with either a digital circuit, or with an analog circuit, such as, for example, an operational amplifier" (page 8 of the Brief), however, the specification only discloses an AND gate circuit 47 for performing an AND function and is implemented with a logical circuit, the specification does not disclose or include **any** analog circuit (such as an operational amplifier as alleged by appellants) which performs an AND function. Appellants argues "that an embodiment of the present invention including an analog circuit which performs an AND function would fall within the scope of independent application

claims 1, 10, and 14-15 and dependent application claims 2-9 and 11-13 depending from independent application claims 1 and 10", however, it is not seen anywhere in the specification or elsewhere in the application that supports appellants' position that the "AND gate 47" is implemented with an analog circuit. Therefore, in light of the specification, both the AND logical circuit in the patented claims and the AND functional circuit in the present claims are directed to the same AND gate circuit 47, there is no any other AND functional circuit (for example, an operational amplifier alleged by the appellants) to perform the AND function other than the AND gate circuit 47. Furthermore, through the specification appellants have never ever used the terms "functional" or "analog" at all, clearly an indication that such was never intended to be in the originally specification and that the use of such terms in the present continuation application is an afterthought. As admitted by appellants on page 7 to page 8 line 7, that the AND logical circuit is a digital circuit in the patent and its specification, therefore the use of the term "functional" in light of the same specification would only lead to one conclusion that the term "functional" is the same as that of "logical" with both referring to the same logical AND gate 47 and no possibility of any other circuits such as analog circuits. Hence, the present claims and the patented claims are directed to the same invention and are properly rejected under 35 U.S.C. 101.

Appellants' remarks regarding MOSFET transistor and a transistor on pages 11 are not persuasive since it is appellants' own interpretation and hence is irrelevant to this application.

Conclusion

For the above reasons, it is believed that the Final rejection under 35 U.S.C. 101 is proper and the Board of Patent Appeals and Interferences is therefore respectfully urged to sustain the Examiner's rejection.

Respectfully submitted,

REGINA LIANG
PRIMARY EXAMINER

Conferees:

Richard Hjerpe (SPE AU 2674)

Steve Saras (SPE AU 2675)